Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Electronics and Communication Engineering

EC8095 – VLSI DESIGN

Unit III - MCQ Bank

1. Inverting dynamic register element consists of _____ transistors for nMOS and _____ for CMOS.

a) Two, three

b) Three, two

c) Three, four

d) Four, three

Answer: c

2. Non inverting dynamic register storage cell consists of _____ transistors for nMOS and _____ for CMOS.

a) Six, eight

b) Eight, six

c) Five, six

d) Six, five

Answer: a

3. Register cell consists of ----------

a) Inverter

b) Pass transistor

c) Inverter & pass transistor

d) None of the mentioned

Answer: c

4. For signals which are updated frequently _____ is used.

a) Static storage

b) Dynamic storage

c) Static and Dynamic storage

d) Buffer

Answer: b

5. In four bit dynamic shift register output is obtained ----------

a) Parallel output at inverters 1, 3, 5, 7

b) Parallel output at inverters 1, 5, 8

c) Parallel output at all inverters

d) Parallel output at inverter 2, 4, 6, 8

Answer: d

6. Clocked sequential circuits are ----------

a) Two phase overlapping clock

b) Two phase non overlapping clock

c) Four phase overlapping clock

d) Four phase non overlapping clock

Answer: b

7. Which circuit converts irregularly shaped waveform to regular shaped waveforms?

a) Schmitt trigger

b) Voltage limiter

c) Comparator

d) None of the mentioned

Answer: a

8. In which configuration a dead band condition occurs in Schmitt trigger ----------

a) Differential amplifier with positive feedback

b) Voltage follower with positive feedback

c) Comparator with positive feedback

d) None of the mentioned

Answer: c

9.- ---------- are the types of reset in sequential circuits.

a) Synchronous

b) Asynchronous

c) Both a and b

d) None of the above

Answer: c

10. In Schmitt trigger responds to a slowly changing input waveform with a fast transition time at the output

a) True

b) False

Answer: a

11. ---------- are refers to temporal variation of the clock period at a given point that is clock period is expand or reduce on a cycle by cycle.

a) Clock Skew

b) Clock rate

c) Clock jitter

d) None of the above

Answer: c

12. Clocks have some uncertainty in their arrival times that can cut into the time available for useful computation ----------

a) Clock Skew

b) Clock rate

c) Clock jitter

d) None of the above

Answer: a

13**.** ---------- new data are applied to a computational circuit in intervals determined by the maximum propagation delay of the computational circuit**.**

a) Synchronous Pipelining

b) Asynchronous Pipelining

c) Both a and b

d) None of the above

Answer: a

14. ---------- new data are applied to a computational circuit in intervals determined by the average propagation delay of the computational circuit.

a) Synchronous Pipelining

b) Asynchronous Pipelining

c) Both a and b

d) None of the above

Answer: b

15. The ability of slow logic in one half cycle to use time normally allocated to faster logic in another half cycle is called ----------

a) Time borrowing

b) Cycle stealing

c) Both a and b

d) None of the above

Answer: c

16. --------- are the methods of sequencing static circuits.

a) Flip flops

b) Pulsed Latches

c) 2 phase transparent latches

d) All of the above

Answer: d

17. The latch that has short clock to Q delay and long hold time is called ----------

a) Pulse latch

b) Flip flop

c) None of the above

d) All of the above

Answer: a

18. The time required for an input data to settle _____ the triggering edge of clock is known as 'Setup Time'.

a. Before

b. During

c. After

d. All of the above

Answer: a

19. Hold time is defined as the time required for the data to _____ after the triggering edge of clock.

a. Increase

b. Decrease

c. Remain stable

d. All of the above

Answer: c

20.Before the commencement of design, the clocking strategy determine/s _____

a. Number of clock signals necessary for routing throughout the chip

b. Number of transistors used per storage requirement

c. Power dissipated by chip & the size of chip

d. All of the above

Answer: d

21. Which sequential circuits generate the feedback path due to the cross-coupled connection from output of one gate to the input of another gate?

a. Synchronous

b. Asynchronous

c. Both

d. None of the above

Answer: b

22.How are the sequential circuits specified in terms of time sequence?

a. By Inputs

b. By Outputs

c. By Internal states

d. All of the above

Answer: d

23.Flip flop samples the input that is changing during its aperture the output Q may take on a voltage between 0 and VDD in a forbidden zone ----------

a) Meta stable

b) A stable

c) Mono stable

d) None of the above

Answer: a

24. A ---------- is a circuit that generates a pulse of predetermined width every time the quiescent circuit is triggered by a pulse or transition event.

a) Meta stable

b) A stable

c) Mono stable

d) None of the above

Answer: c

25.The output oscillates back and forth between two quasi states with apredetermined by the circuit .

a) Meta stable

b) A stable

c) Mono stable

d) None of the above

Answer: b